REMARKS

Claims 1 through 15 are currently pending in the application.

This amendment is in response to the Office Action of January 27, 2004.

35 U.S.C. § 112 Claim Rejections

Claims 10 is rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant has amended the claimed invention as suggested by the Examiner for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claim 10 is allowable under the provisions of 35 U.S.C. § 112.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Yew et al. (U.S. Patent 6,049,129) in view of APA (17)

Claims 1, 4, 5, 7, 9 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. (U.S. Patent 6,049,129) in view of APA (17). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicant asserts that any combination of the Yew et al. reference and APA (17 does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claims 1, 10, and 15 because, at the very least, any combination of the cited prior art fails to teach or suggest all the claim limitations of the presently claimed inventions and any rejection of the inventions of presently amended independent claims 1, 10, and 15 would be a hindsight reconstruction of the presently claimed inventions based solely upon Applicant's disclosure, not the cited prior art as any combination of the cited prior art fails to teach or suggest all the claim limitations of the presently claimed inventions.

Yew et al. describes a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip 50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58, lines 60-62).

APA (17) teaches or suggests, when taken with drawing FIGS. 16 and 18, a technique of face-down attachment of a semiconductor die 232 onto a semiconductor substrate 234 with an adhesive tape 236 has been developed. With this technique, the semiconductor substrate 234 has an opening 238 therethrough with electrical connections 240 (shown as bond wires) extending through the opening 238 to connect the bond pads 242 on an active surface 262 of the semiconductor die 232 to the traces 244 on an active surface 250 of the semiconductor substrate 234. The adhesive tape 236 used in these assemblies is generally narrow and does not extend to an edge 246 of the semiconductor die 232, resulting in exterior voids 248, and does not extend to an edge 252 of the opening 238, resulting in interior voids 254. The opening 238 is filled and

the electrical connections 240 are covered with a glob top material 256 injected into the opening 238, as shown in FIG. 17. Thus, the electrical connections 240 are protected from bond wire sweep and connection detachment. As shown in FIG. 18, an encapsulant material 258 is molded over the semiconductor die 232.

Applicant asserts that any combination of the Yew et al. reference and APA (17) fails to teach or suggest the claim limitations of the presently claimed inventions of presently amended independent claims 1, 10, and 15 calling for "at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of said at least one adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening for substantially preventing damage to a portion of the active surface of the semiconductor die by filler particles in a material used to fill the at least one opening in the substrate being located between the first surface of the substrate and the active surface of the at least one semiconductor die". Any combination of the Yew et al. reference and APA (17) contains no teaching or suggestion whatsoever regarding such claim limitations. The Yew et al. reference is silent regarding any such claim limitations while APA (17) clearly sets forth the prior art having such a problem as Applicant's invention addresses. Therefore, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claims 1, 10, and 15.

Further, Applicants asserts that any rejection of the inventions of presently amended independent claims 1, 10, and 15 would be a hindsight reconstruction of the presently claimed inventions based solely upon Applicant's disclosure, not the cited prior art as any combination of the cited prior art fails to teach or suggest all the claim limitations of the presently claimed inventions. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Further, any such rejection cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claims 1, 10, and 15.

Therefore, Applicant asserts that presently amended independent claims 1, 10, and 15 are allowable over the cited prior art as well as dependent claims 4, through 9 and 11 through 14 therefrom.

Obviousness Rejection Based on Yew et al. (U.S. Patent 6,049,129) in view of APA (Fig. 15 & 17) and Khandros et al. (U.S. Patent 5,148,266)

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. (U.S. Patent No. 6,049,129) in view of APA (15 & 17) and Khandros et al. (U.S. Patent 5,148,266). Applicant respectfully traverses this rejection, as hereinafter set forth.

Again, Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Again, turning to the cited prior art, Yew et al. describes a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip 50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58, lines 60-62).

APA (17) teaches or suggests, when taken with drawing FIGS. 16 and 18, a technique of face-down attachment of a semiconductor die 232 onto a semiconductor substrate 234 with an adhesive tape 236 has been developed. With this technique, the semiconductor substrate 234 has

an opening 238 therethrough with electrical connections 240 (shown as bond wires) extending through the opening 238 to connect the bond pads 242 on an active surface 262 of the semiconductor die 232 to the traces 244 on an active surface 250 of the semiconductor substrate 234. The adhesive tape 236 used in these assemblies is generally narrow and does not extend to an edge 246 of the semiconductor die 232, resulting in exterior voids 248, and does not extend to an edge 252 of the opening 238, resulting in interior voids 254. The opening 238 is filled and the electrical connections 240 are covered with a glob top material 256 injected into the opening 238, as shown in FIG. 17. Thus, the electrical connections 240 are protected from bond wire sweep and connection detachment. As shown in FIG. 18, an encapsulant material 258 is molded over the semiconductor die 232.

The Khandros reference teaches or suggests a semiconductor chip assembly having an interposer and flexible leads (Title). The semiconductor chip is mounted to contact pads in a compact area array. An interposer is disposed between the chip and the substrate. The contacts on the chip are connected to terminals on the interposer by flexible leads that extend through openings in the interposer. (Abstract).

Again, Applicant asserts that any combination of the Yew et al. reference and APA (17) and the Khandros et al reference fails to teach or suggest the claim limitations of the presently claimed inventions of presently amended independent claim 1 from which claims 6 depends through intervening claim 4 calling for "at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of said at least one adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening for substantially preventing damage to a portion of the active surface of the semiconductor die by filler particles in a material used to fill the at least one opening in the substrate being located between the first surface of the substrate and the active surface of the at least one semiconductor die". Any combination of the Yew et al. reference and APA (17) and the Khandros et al. reference contains no teaching or suggestion whatsoever regarding such claim limitation. Both the Yew et al. reference and the Khandros et al. reference are silent regarding any such claim limitations while APA (17) clearly sets forth the prior art having such a problem as Applicant's invention addresses. Therefore, any combination of the cited prior art does not and cannot

establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 1 as well as dependent claim 6 therefrom.

Further, Applicants asserts that any rejection of the inventions of presently amended independent claim 1 and dependent claim 6 therefrom would be a hindsight reconstruction of the presently claimed inventions based solely upon Applicant's disclosure, not the cited prior art as any combination of the cited prior art fails to teach or suggest all the claim limitations of the presently claimed inventions. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Further, any such rejection cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claims 1 and dependent claim 6 therefrom.

Therefore, Applicant asserts that presently amended independent claim 1 and dependent claim 6 therefrom are allowable over any combination of the cited prior art.

Obviousness Rejection Based on Yew et al. (U.S. Patent 6,049,129) in view of APA (Fig. 17) and further in view of Murakami et al. (U.S. Patent 5,612,569)

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. (U.S. Patent 6,049,129) in view of APA (17) and further in view of Murakami et al. (U.S. Patent 5,612,569). Applicant respectfully traverses this rejection, as hereinafter set forth.

Again, Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Again, turning to the cited prior art, Yew et al. describes a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip

50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58, lines 60-62).

APA (17) teaches or suggests, when taken with drawing FIGS. 16 and 18, a technique of face-down attachment of a semiconductor die 232 onto a semiconductor substrate 234 with an adhesive tape 236 has been developed. With this technique, the semiconductor substrate 234 has an opening 238 therethrough with electrical connections 240 (shown as bond wires) extending through the opening 238 to connect the bond pads 242 on an active surface 262 of the semiconductor die 232 to the traces 244 on an active surface 250 of the semiconductor substrate 234. The adhesive tape 236 used in these assemblies is generally narrow and does not extend to an edge 246 of the semiconductor die 232, resulting in exterior voids 248, and does not extend to an edge 252 of the opening 238, resulting in interior voids 254. The opening 238 is filled and the electrical connections 240 are covered with a glob top material 256 injected into the opening 238, as shown in FIG. 17. Thus, the electrical connections 240 are protected from bond wire sweep and connection detachment. As shown in FIG. 18, an encapsulant material 258 is molded over the semiconductor die 232.

Murakami teaches or suggests a semiconductor device having bonding wires 5 covered with a flexible/fluid substance 20. Mold resin 2A covers flexible/fluid substance 20. The mold resin 2A is bored with a hole 22 at the side opposite to the principal surface of the semiconductor chip 1 to expose a portion of the semiconductor chip 1 to the outside. (FIG. 34, Col. 31, lines 13-17).

Again, Applicant asserts that any combination of the Yew et al. reference and the Murakami reference and APA (17) fails to teach or suggest the claim limitations of the presently

claimed inventions of presently amended independent claim 1 from which claims 8 depends through intervening claims 4 and 7 calling for "at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of said at least one adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening for substantially preventing damage to a portion of the active surface of the semiconductor die by filler particles in a material used to fill the at least one opening in the substrate being located between the first surface of the substrate and the active surface of the at least one semiconductor die". Any combination of the Yew et al. reference and APA (17) and the Murakami reference contains no teaching or suggestion whatsoever regarding such claim limitation. Both the Yew et al. reference and the Murakami reference are silent regarding any such claim limitations while APA (17) clearly sets forth the prior art having such a problem as Applicant's invention addresses. Therefore, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 1 as well as dependent claim 8 therefrom.

Further, Applicants asserts that any rejection of the inventions of presently amended independent claim 1 and dependent claim 8 therefrom would be a hindsight reconstruction of the presently claimed inventions based solely upon Applicant's disclosure, not the cited prior art as any combination of the cited prior art fails to teach or suggest all the claim limitations of the presently claimed inventions. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Further, any such rejection cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 1 and dependent claim 8 therefrom.

Therefore, Applicant asserts that presently amended independent claim 1 and dependent claim 6 therefrom are allowable over any combination of the cited prior art.

Obviousness Rejection Based on Yew et al. (U.S. Patent 6,049,129) in view of APA (Fig. 17) and further in view of Boyko et al. (U.S. Patent 5,784,782)

Claims 11 through 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. (U.S. Patent 6,049,129) in view of APA (17) and further in view of Boyko et al. (U.S.

Patent 5,784,782). Applicant respectfully traverses this rejection, as hereinafter set forth.

Yet again, Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Yet again, turning to the cited prior art, Yew et al. describes a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip 50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58, lines 60-62).

APA (17) teaches or suggests, when taken with drawing FIGS. 16 and 18, a technique of face-down attachment of a semiconductor die 232 onto a semiconductor substrate 234 with an adhesive tape 236 has been developed. With this technique, the semiconductor substrate 234 has an opening 238 therethrough with electrical connections 240 (shown as bond wires) extending through the opening 238 to connect the bond pads 242 on an active surface 262 of the semiconductor die 232 to the traces 244 on an active surface 250 of the semiconductor substrate 234. The adhesive tape 236 used in these assemblies is generally narrow and does not extend to an edge 246 of the semiconductor die 232, resulting in exterior voids 248, and does not extend to

an edge 252 of the opening 238, resulting in interior voids 254. The opening 238 is filled and the electrical connections 240 are covered with a glob top material 256 injected into the opening 238, as shown in FIG. 17. Thus, the electrical connections 240 are protected from bond wire sweep and connection detachment. As shown in FIG. 18, an encapsulant material 258 is molded over the semiconductor die 232.

Boyko teaches or suggests a method for fabricating printed circuit boards with cavities. The printed circuit board 10 has a dielectric layer 12 with metalizations 14 and 16 on both surfaces. (FIG. 1). The printed circuit board may have an additional dielectric layer 22, also with metalizations 24and 26 on both surfaces. (FIG. 1). A window 30 is cut in dielectric layer 22 to form a cavity 31. (FIG. 1). Sticker/adhesive sheet 40, which may be epoxy-glass or "pre-preg" is located between metallized dielectric sheets 12 and 22. (Col. 3, lines 35-38). Sticker/adhesive sheet 40 is designed for high flow when heat and pressure are applied. A window 44 is cut in sticker/adhesive sheet 40 and this window registers with window 30 in dielectric layer 22. (Col. 3, lines 38-44). A release layer 50 is placed on top of metallized dielectric layer 22. Layer 50 is highly stretchable and conformable. (Col. 3, lines 45-48). A sheet 60 of plug material 61 is laid on top of release layer 50. At room temperature, the plug material is pliable enough to tightly conform to cavity 31 and seal in sticker/adhesive sheet 40. (Col. 3, lines 60-62). Another non-melting release layer 70 is laid over sheet 60. Next, a breather layer 74 is laid over release layer 70. The resulting structure is sealed in a nylon bag, the bag is evacuated, and subjected to heat and pressure. (Col. 4, lines 21-29). When the release layer 70, sheet 74, are removed the resulting structure has the sticker/adhesive sheet bound ground plane 16 to metallized dielectric layer 22. The sticker/adhesive material has flowed within the cavity 31, creating a fillet 82 of the sticker/adhesive sheet material along the bottom perimeter of the cavity. (Col. 4, lines 32-39).

Applicant respectfully submits that Yew and Boyko and APA (17) fail to teach or suggest elements of claims 11 through 14 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the elements of the claimed invention of a semiconductor die assembly that includes "at least one fillet located proximate said at least one adhesive tape and said edge of said at least one semiconductor die" of claim11; "at least one fillet located proximate said at least one adhesive tape and said edge of said at least one semiconductor substrate opening" of claim 12; "at least one fillet located proximate said at least one adhesive tape and said active surface of said at least one semiconductor die" of claim 13; and "at least one fillet located proximate said at least one adhesive tape and said semiconductor substrate first surface" of claim 14. Yew and APA (17) do not teach fillets. Boyko teaches fillets within a cavity formed in layers of a printed circuit board. The fillet material of Boyko is heated to liquify and settle at the bottom of the cavity to form fillets. Boyko does not teach or suggest that the fillet is proximate to adhesive tape, edge of semiconductor die, or substrate opening. Any semiconductor device mounted to the printed circuit board of Boyko would not be proximate to the fillets formed during the printed circuit board fabrication process since the fillets are formed at the bottom of the cavity, away from the mounting surface.

In addition, the references themselves teach away from the proposed combination and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention since Boyko is directed toward producing a printed circuit board with cavity. Yew teaches a chip size integrated package. It would not be obvious to combine a method for producing printed circuit board with cavities and a method for producing chip scale packages. Printed circuit board fabrication requires higher temperatures and pressures that would damage or destroy semiconductors.

Accordingly, any combination of Yew and Boyko and APA (17) cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Again, Applicant asserts that any combination of the Yew et al. reference and the Boyko reference and APA (17) additionally fails to teach or suggest the claim limitations of the presently claimed inventions of presently amended independent claim 1 from which claims 11 through 14 depend calling for "at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of said at

least one adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening for substantially preventing damage to a portion of the active surface of the semiconductor die by filler particles in a material used to fill the at least one opening in the substrate being located between the first surface of the substrate and the active surface of the at least one semiconductor die". Any combination of the Yew et al. reference and the Boyko reference and APA (17) contains no teaching or suggestion whatsoever regarding such claim limitation. Both the Yew et al. reference and the Boyko reference are silent regarding any such claim limitations while APA (17) clearly sets forth the prior art having such a problem as Applicant's invention addresses. Therefore, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 1 as well as dependent claims 11 through 14 therefrom.

Further, Applicants asserts that any rejection of the inventions of presently amended independent claim 1 and dependent claims 11 through 14 therefrom would be a hindsight reconstruction of the presently claimed inventions based solely upon Applicant's disclosure, not the cited prior art as any combination of the cited prior art fails to teach or suggest all the claim limitations of the presently claimed inventions. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and, clearly, improper. Further, any such rejection cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claims 1 and dependent claims 11 through 14 therefrom.

Therefore, Applicant asserts that presently amended independent claim 1 and dependent claims 11 through 14 therefrom are allowable over any combination of the cited prior art.

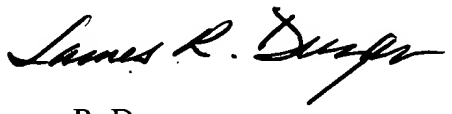
Allowable Subject Matter

Claims 2 and 3 are allowed.

Applicant submits that claims 1 through 15 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 and 4 through 15 and the case passed for issue.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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